Printed Page:- Subject Code:- AEC0502

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: V - THEORY EXAMINATION (2023 - 2024)

Subject: CMOS Digital Integrated Circuit

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A 20

1. Attempt all parts:-

1-a. What does MOSFET stands for? (CO1) 1

(a) Metal Oxide Semiconductor Field Effect Transistor

(b) Modern Oxidized Silicon based Field Effect Transistor

(c) Modern Oxidized Silicon based Force Effect Transistor

(d) Metal Oxide silicon Field Equivalent Transistor

1-b. _____ is normally referred to as ON switches. (CO1) 1

(a) JFET

(b) UJT

(c) Depletion MOSFET

(d) Enhancement MOSFET

1-c. _____ can pass a logic 1 perfectly, but cannot pass a logic 0 perfectly. (CO2) 1

(a) NMOS transistor

(b) PMOS transistor

(c) CMOS transistor

(d) None of these

1-d. _____ can pass a logic 0 perfectly, but cannot pass a logic 1 perfectly. (CO2) 1

(a) NMOS transistor

(b) PMOS transistor
(c) CMOS transistor
(d) None of these

1-e. Switch logic is based on _____ . (CO3) 1

(a) Pass transistors
(b) Transmission gates
(c) Pass transistors and Transmission gates
(d) Design rules

1-f. In Pseudo-nMOS logic, n transistor operates in (CO3) 1

(a) Cut-off region
(b) Saturation region
(c) Resistive region
(d) Non saturation region

1-g. Circuit designers need _____ circuits. (CO4) 1

(a) tighter
(b) smaller layout
(c) decreased silicon area
(d) all of the mentioned

1-h. Hierarchical decomposition of a large system in VLSI design is called…….. (CO4) 1

(a) Modularity
(b) Regularity
(c) Locality
(d) Decomposability

1-i. An ASIC stands for _____ . (CO5) 1

(a) American Specific Instruction code
(b) Application Specific Integrated Circuit
(c) Application Specific Instruction Code
(d) American Standard input Code

1-j. Which Hardware description language is used for ASICs? (CO5) 1

(a) system Verilog
(b) system c
(c) C++
(d) verilog

2. Attempt all parts:-

2.a. Why is MOSFET a voltage controlled device? (CO1) 2

2.b. Draw the truth table of half-adder. (CO2) 2

2.c. What are transmission gates? (CO3) 2

2.d.	What do you understand by design hierarchy in VLSI? (CO4)	2
2.e.	What are the goals of floorplanning? (CO5)	2

SECTION-B 30

3. Answer any five of the following:-

3-a.	Differentiate the enhancement-type and depletion-type MOSFET. (CO1)	6
3-b.	Derive the expression for drain current in linear region of MOSFET. (CO1)	6
3-c.	Explain multiplexer and demultiplxer circuits. (CO2)	6
3-d.	What are the applications of sequential circuits? (CO2)	6
3.e.	Realize the OR and NOR logic functions using differential CMOS logic. (CO3)	6
3.f.	Define Hierarchy by taking the example of 16 bit full adder. (CO4)	6
3.g.	Draw and explain in brief the ASIC design flow. (CO5)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	What do you mean by drain-induced barrier lowering (DIBL)? Explain with the help of diagram. (CO1)	10
4-b.	Why scaling is required in VLSI chips? And also explain different scaling methods of MOSFET. (CO1)	10

5. Answer any one of the following:-

5-a.	Derive the expression for sum and carry output of full adder using truth table and realize the full adder circuit using CMOS logic. (CO2)	10
5-b.	Design 4:1 multiplexer using complementry CMOS logic. (CO2)	10

6. Answer any one of the following:-

6-a.	Realize the function $F = A' + BC'$ using pass-transistor logic circuits. Why is it necessary to restore the output voltage level of a pass-transistor circuit? (CO3)	10
6-b.	Draw and explain the operation of domino CMOS logic based 4-input NAND gate. Briefly mention the advantages and disadvantages of domino CMOS logic over static CMOS logic. (CO3)	10

7. Answer any one of the following:-

7-a.	Draw the flow chart of VLSI Design flow and explain the operation of each step in detail. (CO4)	10
7-b.	Explain the detailed logic configurable block Architecture of FPGA. (CO4)	10

8. Answer any one of the following:-

8-a.	Explain in detail the steps involved in ASIC design. (CO5)	10
8-b.	Explain in detail the goals and objectives of placements also discuss the i/p's and o/p's of placement? (CO5)	10